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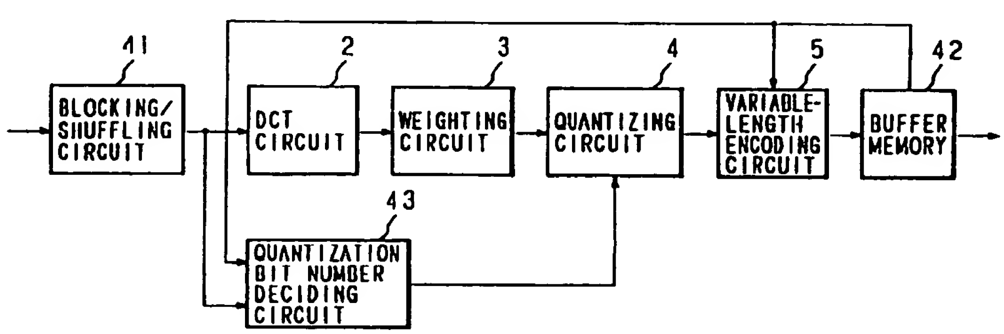
(54) Video signal encoding apparatus using a block shuffling technique

(57) A video signal encoding apparatus for compressing and encoding a digital video signal comprises block structuring means (41) for structuring the video signal into a matrix array of blocks, transformation means (2) for performing an orthogonal transform on each of the structured blocks, and encoding means (5), wherein unit structuring means (41) for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, by shuffling the blocks in such a manner that any given shuffling unit and four shuffling units most adjacent to said given shuffling unit belong to different units.

FIG. 14



EP 0 806 872 A2

Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a video signal encoding apparatus for compressing and encoding a video signal by dividing it into blocks and performing an orthogonal transform on each block.

Description of the Prior Art

If video data converted to digital signals is directly recorded on tape or other recording medium, the volume of data will be so great that it will usually exceed the limit of the data amount that the recording medium can hold. Therefore, when recording a digital video signal on tape or other recording medium, it is necessary to compress it so that the data volume does not exceed the limit. To achieve this, it has been known to compress the video signal by using a high-efficiency encoding apparatus.

One example of such high-efficiency encoding that has been widely used is the orthogonal transform encoding method in which transform coefficients obtained by orthogonal-transforming the original signal are quantized for encoding. This method is known to provide high encoding efficiency. In encoding a video signal by this method, the video signal is first divided into blocks each consisting of n × n pixels (where n is an integer), an orthogonal transformation is performed on each block to transform it into a transform coefficient representing n × n frequency regions, and then the transform coefficient is quantized. However, when all blocks are quantized with the same number of bits, adequate image quality can be obtained for the video blocks in flat areas, but noise appears in the video blocks including edge areas since errors are dispersed in the vicinity of the edge areas.

An example of an encoding apparatus that overcomes the above problem is disclosed in Japan Patent Application Laid-Open No.2-105792. Fig.1 shows a block diagram of the encoding apparatus disclosed in the Patent Publication. The encoding apparatus shown is described below with reference to Fig.1. A video signal is inputted to a blocking circuit 51 where it is divided into blocks, each block then being supplied to an orthogonal transforming circuit 52 for orthogonal transformation. The transform coefficient obtained by the orthogonal transformation is quantized by a quantizing circuit 53. The quantizing circuit 53 has the ability to perform quantization using a variable number of quantization bits. An edge area detecting circuit 54 is provided to detect the edges of the video signal, while a flat area detecting circuit 55 is provided to determine whether the block represents a flat area. Based on the outputs from the edge area detecting circuit 54 and the flat area detecting circuit 55, a block identifying circuit 56 determines whether the block includes an edge area as well as a flat area, the result of which is fed to the quantizing circuit 53 to determine the number of quantization bits. When the whole block is flat or when the whole block has a complicated structure, it is decided to use a smaller bit code for quantization since noise is not appreciably visible. On the other hand, if the block includes an edge area as well as a flat area, it is decided to use a higher bit code for quantization to prevent the generation of noise in the flat area. Thus, in the encoding apparatus disclosed in the above Patent Publication, in order to overcome the aforementioned problem, the transform coefficients for blocks including both edge and flat areas are quantized using a higher bit code to reduce the noise and thereby improve the image quality after decoding. The determining factors used to detect the edge or flat areas in a block include a variance within the block, the maximum value of the block, the dynamic range of the block, etc. These factors are collectively referred to as the activity index. In the above prior art encoding apparatus, the number of quantization bits (quantization level) is selected for each block on the basis of the activity index.

The output of the quantizing circuit 53 of Fig.1 is encoded, usually using entropy encoding such as Huffman encoding, into a variable-length code for transmission. The hit length of one block after variable-length encoding varies from block to block, and in the case of a recording medium such as a helical scan digital video tape recorder (VTR) having a fixed track length, it is convenient to grasp the number of data blocks to be recorded per track. Therefore, it is a usual practice to predetermine at least the number of data blocks to be recorded per track. Also, when block correcting codes (e.g., BCH codes, Reed-Solomon codes, etc.) are employed as error-correcting codes, it may be practiced to fix the data length of variable-length code for each error-correcting block. Usually, in encoding of video signals, one field or frame is divided into N segments (where N is an integer), each segment serving as a unit, and the maximum data amount is set for each of the N units.

However, in a channel, such as a digital VTR, in which the data length for the variable-length codes is fixed, the data length of variable-length code may vary from code.to code after variable-length encoding depending on the kind of the image processed, and the total code length after variable-length encoding may exceed the fixed length of the channel, resulting in an overflow. If this happens, the transmission will be cut off because of dataflow, and therefore, not only overflown data but also the subsequent data will not be transmitted. This presents the problem of an inability to correctly perform the decoding of the original signal.

Variable-length encoding of a television image is usually performed in sequence from left to right and from top to bottom of the television screen. Therefore, the problem is that the above-mentioned cutoff is likely to occur in the center of the television screen where the feature elements of the image are contained.

IEEE TRANSACTIONS ON ACOUSTICS AND SPEECH AND SIGNAL PROCESSING; vol. 37, no. 11, November 1989, NY, US, pages 1743-1749, NGAN et al.: "Adaptive Cosine Transform Coding of Images in Perceptual Domain" already discloses a video signal encoding apparatus for compressing and encoding a digital video signal to obtain coded data compressed within a predetermined data amount. This apparatus comprises means for structuring blocks each consisting of a plurality of pixels in the video signal, means for performing an orthogonal transformation on each of the structured blocks to obtain a transform coefficient, means for quantizing the transform coefficient, means for encoding the quantized data to obtain coded data, means for storing the obtained coded data, and means for controlling the quantizing means on the basis of the amount of the coded data stored in the storage means.

PAJP, vol. 12, no. 124 (E 601) shows a picture signal transmission system which obtains a smooth reproducing moving image with improved visual characteristic by dividing both surfaces into plural areas, applying priority to the respective areas and transmitting more information of the area of the higher priority than the information of the area of the lower priority.

PAJP. vol. 12, no. 355 (E 661) describes a picture compressing device which in order to reduce the number of quantizing errors and to shorten the operating time comprises a preprocessing means which preprocesses original picture data and a rearranging section which rearranges an orthogonally transformed output in blocks of the same frequency component.

Further, EP-A-0 322 955 refers to a receiver for a high definition television signal in which the signal prior to transmission is sub-sampled on a block-by-block basis according to the movement. The received sub-sampled signal is applied to a shuffler which shuffles the pixels of blocks in a manner which is the inverse to that performed prior to transmission.

SUMMARY OF THE INVENTION

It is the object of the invention to provide a video signal encoding apparatus capable of fixing the encoded data length to a predetermined length wherein distortions resulting from transmission cutoffs are not easily visible even when the code length of the data to be transmitted is fixed.

According to a first embodiment of the present invention a video signal encoding apparatus for compressing and encoding a digital video signal containing a chrominance signal comprises block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality of pixels, transformation means for performing an orthogonal transform on each of the structured blocks to obtain a transform coefficient, encoding means for encoding the obtained transform coefficient to obtain coded data, and unit structuring means for structuring units each comprising a plurality of block, prior to the orthogonal transform by said transformation means, by shuffling the blocks in such a manner that any given shuffling unit and four shuffling units most adjacent to said given shuffling unit belong to different units, the reference of the shuffling unit being the size that the blocks of said chrominance signal occupy on the screen.

According to a second embodiment of the present invention a video signal encoding apparatus for compressing and ancoding a digital video signal comprises block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality of pixels, transformation means for performing an orthogonal transform on each of the structured blocks to obtain a transform coefficient, encoding means for encoding the obtained transform coefficient to obtain coded data, and unit structuring means for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, in such a manner that any given block and four blocks most adjacent to said given block belong to different units.

According to a third embodiment of the present invention a video signal encoding apparatus for compressing and encoding a digital video signal comprises block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality or pixels, transformation means for prerforming an orthogonal transform on each of the structured blocks to obtain a transform coefficient, encoding means for encoding the obtained transform coefficient to obtain coded data, unit structuring means for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, in such a manner that any given block and four blocks most adjacent to said given block belong to different units, decision means for deciding the order in which the blocks are to be encoded, the order within each unit being such that encoding is performed starting with the blocks nearer to the center of the screen and then proceeding to the blocks nearer to the sides of the screen, and control means for controlling the amount of coded data on a unit-by-unit basis.

The above and further objects and features of the invention will more fully be apparent from the following detailed description with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the configuratin of a prior art video signal encoding apparatus.

Fig. 2 is a diagram showing the configuration of a video signal encoding apparatus comprising a variable length encoding circuit and a buffer memory.

Fig. 3 is a diagram showing an example of encoding during the process.

Fig. 4 is a diagram showing the scanning sequence during encoding.

Fig. 5 is a diagram showing an alternative configuration of the apparatus of Fig. 2.

Fig. 6 is a diagram showing the configuration of a video signal encoding apparatus in accordance with a first embodiment of the invention.

Fig. 7 is a diagram explaining the operation of shuffling in the first embodiment.

Fig. 8 is a diagram explaining the principle of shuffling in the first embodiment.

Fig. 9 is a diagram showing an example of shuffling in the first embodiment.

Fig. 10 is a diagram showing another example of shuffling in the first embodiment.

Fig. 11 is a diagram showing still another example of shuffling in the first embodiment.

Fig. 12 is a diagram showing the configuration of a shuffling circuit in the first embodiment.

Fig. 13 is a diagram showing the configuration of a video signal encoding apparatus in accordance with a second embodiment of the invention.

Fig. 14 is a diagram showing an alternative configuration of the second embodiment.

Fig. 15 is a diagram showing an example of shuffling in the second embodiment.

Fig. 16 is a diagram showing another example of shuffling in the second embodiment.

Fig. 17 is a diagram showing still another example of shuffling in the second embodiment.

Fig. 18 is a diagram showing yet another example of shuffling in the second embodiment.

Fig. 19 is a diagram showing a further example of shuffling in the second embodiment.

Fig. 20 is a diagram showing a still further example of shuffling in the second embodiment.

In Fig. 2, the reference numeral 1 indicates a blocking circuit for dividing the input digital video signal into blocks each consisting of plurality of pixels. Each block is fed from the blocking circuit 1 to a DCT circuit 2. The DCT circuit 2 performs a discrete cosine transform (DCT) on each block and supplies the obtained transform coefficient (DCT coefficient) to a weighting circuit 3. The weighting circuit 3 performs a weighting to each DCT coefficient and supplies the weighted DCT coefficient to a quantizing circuit 4. The quantizing circuit 4 quantizes the weighted DCT coefficient with the number of quantization bits determined by a controller 8, and supplies the quantized DCT coefficient to a variable-length encoding circuit 5 through a switch 7. The variable-length encoding circuit 5 encodes the quantized DCT coefficient into a variable-length code and transfers the variable-length encoded data to a buffer memory 6. The buffer memory 6 is constructed from a RAM or the like and has the storage capacity equivalent to the data length of one track. The switch 7 turns on and off the data input to the variable-length circuit 5. The controller 8 controls the number of quantization bits for the quantizing circuit 4, as well as the switching operation of the switch 7, on the basis of the amount of data stored in the buffer memory 6.

The operation will now be described.

The data obtained by sampling the video signal is divided by tie blocking circuit 1 into blocks each consisting of, for example, eight pixels in both horizontal and vertical directions. The DCT circuit 2 performs a DCT on each block, and the obtained DCT coefficient is then performed a weighting by the weighting circuit 3. At this time, the weighting is performed so that weighting factors for DCT coefficients in higher frequency regions will be smaller values. This is because the visual resolution drops for higher frequency regions, allowing high-efficiency encoding without noticeable degradation. Next, the weighted DCT coefficient is quantized by the quantizing circuit 4. Quantized n-bit data may be expressed as shown in Fig.3, for example. This data is encoded by the variable-length encoding circuit 5 into a variable-length code by performing one-dimensional scanning as shown in Fig.4. The variable-length encoding circuit 5 is a circuit for encoding data into a code whose length depends, for example, on the string of zeros (zero run length) and nonzero value, and usually, the Huffman encoding and like methods are widely used. The output of the variable-length encoding circuit 5 is stored in the buffer memory 6 for transfer to the transmission channel.

However, the length of the variable-length code outputted from the variable-length encoding circuit 5 varies according to the image pattern and, depending on the situation, may exceed or may not reach the maximum transmissible code length. The controller 8 predicts an occurrence of excess data by comparing the address value being written in the buffer memory 6 with the limit data length, and outputs signals to control the number of quantization bits for the quantizing circuit 4 and the switching operation of the switch 7.

Therefore, even if the data volume instantaneously increases at a particular portion of the image on the television screen, the buffer memory 6 can provide a sufficient capacity for data storage, and there arises no situation that results in an overflow or that causes the controller 8 to direct transmission cutoff.

Fig.5 is a block diagram showing an alternative configuration. In this alternative configuration, the controller 8 con-

trols only the switching operation of the switch 7.

The preferred embodiments of the present invention will now be described with reference to the accompanying drawings.

(Embodiment 1)

When a plurality of blocks is grouped into a unit, it has been a usual practice to perform encoding unit by unit starting from a particular position on the screen (e.g. from the upper left of the screen). Therefore, the code amount varies largely from unit to unit, and there arises the problem that the transmission efficiency decreases when the upper limit of data amount is set to match the units having a larger code amount. The fifth embodiment and the subsequent sixth embodiment of the invention are provided aiming at overcoming such a problem.

Fig. 6 is a block diagram showing the configuration of a video signal encoding apparatus in accordance with the fifth embodiment of the invention. In Fig. 6, the reference numerals 2, 3, 4, and 5 designate a DCT circuit, a weighting circuit, a quantizing circuit, and a variable-length encoding circuit, respectively. These circuits are identical to those shown in Fig.5. At the front stage of the DCT circuit 2, there is provided a blocking/shuffling circuit 41 for dividing a digital video into blocks of a plurality of pixels and shuffling the thus obtained blocks. The block data is supplied from the blocking/shuffling circuit 41 to the DCT circuit 2. The quantizing circuit 4 quantizes the weighted DCT coefficient with the number of quantization bits decided by a quantization bit number deciding circuit 43 and supplies the quantized DCT coefficient to the variable-length encoding circuit 5. The variable-length encoding circuit 5 encodes the quantized DCT coefficient. into a variable-length code and supplies the variable-length code data to a buffer memory 42.

The operation will now be described.

A digital video signal is inputted in scanning line sequence to the blocking/shuffling circuit 41 where the signal is divided into blocks of n × n pixels within one field or one frame and then shuffled in accordance, for example, with the shuffling format shown in Fig.7. One block in Fig. 7 corresponds to one DCT block and the outer frame corresponds to that of the television screen. When the luminance signal conforming to the NTSC system is sampled at a rate of 13.5MHz, for example, the effective scanning area per frame covers 720 pixels in the horizontal direction and 486 pixels in the vertical direction. When one frame is divided into blocks of 8 × 8 pixels, for example, there remain six pixels each in the vertical direction; therefore, it is supposed here to encode the picture signal for 720 × 480 pixels, discarding the data for the three horizontal scanning lines from the top and bottom of the screen. Since the video signal is divided into blocks of 8 × 8 pixels, this means 90 × 60 blocks, i.e., 5,400 blocks in total. That is, when the block address in the horizontal direction within one frame is denoted as i and that in the vertical direction as j, i is expressed as $1 \leq i \leq 90$ and j as $1 \leq j \leq 60$.

Furthermore, the 5,400 blocks are grouped into N units. In Fig. 7, N = 5, and the alphabetic characters in A1, B1, etc. assigned to each block indicate the names of the units. Since N = 5, there are five unit names A to E. The numeric parts in A1, B1, etc. are numbers indicating the encoding sequence within each unit.

In Fig.7, encoding is performed, as a general rule, from left to right and from top to bottom of the screen. In the example shown, since there are 90 blocks in the horizontal direction, the second line from top in Fig.7 begins with the number 19 which is given by dividing 90 by N (= 5) and adding 1 to the quotient. Therefore, the block address (i, j) for the kth encoding in the uth unit can be expressed by the following equation (1) (provided that (1, 1) indicates the top left corner of the screen and (90. 60) the bottom right corner). .pa

$$\left.\begin{aligned} i &= N \times \mathrm{mod}\left(k-1, \frac{90}{N}\right) \\ &\quad + \mathrm{mod}\left(u + \left[\frac{(k-1) \times N}{90}\right] - 1,\ N\right) + 1 \\ j &= \left[\frac{(k-1) \times N}{90}\right] + 1 \end{aligned}\right\} \quad \ldots (1)$$

[a]: Largest integer not exceeding a

For example, when u = 2 and k = 20, the block address is given by:

$$i = 5 \times \mathrm{mod}(20 - 1,\ 18) + \mathrm{mod}\,[2 + [(19 \times 5)/90] - 1,\ 5] + 1 = 5 \times 1 + \mathrm{mod}(2,\ 5) + 1 = 5 + 2 + 1 = 8$$

$$j = [(19 \times 5)/90] + 1 = 2$$

Thus, the block address (8, 2) is obtained. Also, u = 2 indicates the unit name is B, and in Fig. 7, the address (8, 2) designates the block B20. Likewise, the address of the block C57, for example, can be found as follows:

$$i = 5 \times \text{mod}(57 - 1, 18) + \text{mod}\,[3 + [(56 \times 5)/90) - 1, 5] + 1 = 5 \times 2 + \text{mod}(3 + 3 - 1, 5) + 1 = 10 + 0 + 1 = 11$$

$$j = 4$$

which gives the address (11, 4). That is, Fig.7 shows the arrangement of blocks after performing shuffling as expressed by the equation (1).

After the above shuffling, each block is sequentially fed to the DCT circuit 2 for a DCT transform and is then performed a weighting by the weighting circuit 3. The quantization bit number deciding circuit 43 calculates the activity index of each block, on the basis of which the number of quantization bits is decided for the block, the information being fed to the quantizing circuit 4. The weighted DCT coefficient is quantized by the quantizing circuit 4 using the number of quantization bits thus decided, and the quantized data is then encoded by the variable-length encoding circuit 5 using such methods as Huffman encoding, the encoded data being transferred to the buffer memory 42 for storage therein.

As the above shuffling, the patterns represented by the blocks to be coded are randomly dispersed, and therefore, the code length is equalized between the units when the number of blocks is greater than a certain degree. According to the simulation conducted by the inventor, it has been found that, when the units are assigned by shuffling as shown in Fig. 7, the dispersion value indicating the dispersion of the code amount is reduced to 1/5 to 1/10, compared to when a particular position on the screen is grouped together in a unit without shuffling.

Next, the features of this shuffling will be considered. When considering the effects that the shuffling has on the code amount, the point is to avoid concentrating the blocks of the same pattern in the same unit, which leads to the following point when considered in conjunction with pixels. Blocks neighboring an attention block often have similar patterns, therefore, processing is performed to assign neighboring blocks to different units. This processing is described below using the concept of neighborhood.

Each of the nine squares in Fig. 8 represents a DCT block. There are eight blocks (A to F in Fig. 8) that neighbors an attention block. These blocks are referred to as the eight neighboring blocks, of which the four blocks A, B, C, and D that are most adjacent to the attention block are called the four neighboring blocks. Referring back to Fig. 7, it can be seen that when attention is given to a given block, none of its four neighboring blocks belong to the same unit as the attention block. Of its eight neighboring blocks, there are only two blocks that belong to the same unit. The four neighboring blocks that are spatially most adjacent to the attention block are thus made to belong to different units in order to prevent similar patterns from being concentrated in one unit. This serves to equalize the code amount.

This effect can be achieved not only by the equation (1) but by many other methods. Figs. 9 to 11 show only a few examples of the many methods. In the examples of shuffling shown in Figs. 9 to 11, there are no four neighboring blocks that belong to the same unit. The block address (i, j) in Fig. 9 is expressed by the following equation. .pa

$$i = [\frac{\text{mod}(k - 1, 90)}{N}] \times N + [\frac{N + 1}{2}] + (-1)^{\text{mod}(k, N)} \times [\frac{\text{mod}(k, N)}{2}]$$

$$j = \text{mod}(\text{mod}(k - 1, 90) + u - 1, N) + 1 + N \times [\frac{k - 1}{90}]$$

For example, to find the address of the block D98, since u = 4 and k = 98,

$$i = [\{\text{mod}(97, 90)\}/5] \times 5 + 3 + (-1)^{3} \times [\{\text{mod}(98, 5)\}/2] = 5 + 3 - 1 = 7$$

$$j = \text{mod}\,(7 + 4 - 1, 5) + 1 + 5 \times 1 = 0 + 1 + 5 = 6$$

which gives the address (7, 6). The block address (i, j) in Fig. 10 is expressed by the following equation.

$$i = \text{mod}(\text{mod}(k - 1, 90) + u, N) + [\frac{\text{mod}(k - 1, 90)}{N}] \times N$$

$$j = [\frac{k - 1}{90}] \times N + [\frac{N + 1}{2}] + (-1)^{\text{mod}(k-1, N)} \times [\frac{\text{mod}(\text{mod}(k - 1, 90), N) + 1}{2}]$$

For example, to find the address of the block E102, since u = 5 and k = 102,

$$i = \mathrm{mod}(11 + 5, 5) + [11/5] \times 5 = 1 + 10 = 11$$

$$j = 1 \times 5 + 3 + (-1) \times [[\mathrm{mod}(11, 5) + 1]/2] = 5 + 3 - 1 = 7$$

which gives the address (11, 7). Likewise, there exists an equation that realizes the shuffling shown in Fig. 11, along with various other equation that achieve various other shuffling formats.

The circuit that performs the above shuffling operations can be implemented in the configuration shown in Fig. 12. In the figure, the reference numeral 46 designates a block address calculating circuit for calculating the block horizontal address (i) and the block vertical address (j) using the above given equations, and the block address obtained by the block address calculating circuit 46 is supplied to a write/read address generating circuit 45. On the basis of the supplied block address, the write/read address generating circuit 45 outputs a writw/read address to a RAM 44. In the RAM 44, each block is arranged according to the address, thus achieving the shuffling as shown in Figs. 7, 9, 10, and 11.

(Embodiment 2)

With the above shuffling, the code amount is substantially equalized between the units within one field or one frame, but in the case of a time-varying image, the image pattern may completely change after several seconds, causing the code amount of each unit within one field or one frame to increase or decrease. If the code amount increases, in each unit, it may exceed the maximum transmissible data amount. This presents a serious problem, particularly in the case of a helical scan VTR, since, as previously described, each track is divided into lengths so that each length is the result of dividing the track length by an integer, each limited fixed amount being assigned to codes for a fixed number of blocks. The second embodiment of the invention is devised to overcome this problem. The following describes the second embodiment.

Figs. 13 and 14 are block diagrams each showing the configuration of a video signal encoding apparatus in accordance with the second embodiment. In Fig.13, the quantizing circuit 4 and the variable-length encoding circuit 5 are controlled using the information on the memory usage in the buffer memory 42. In Fig.14, the quantization bit number deciding circuit 43 and the variable-length encoding circuit 5 are controlled using the information on the memory usage in the buffer memory 42.

The buffer memory 42 has the capacity to store data of the volume that matches the limit code amount. When the buffer memory 42 nears its full capacity, the probability increases that codes will be generated that may exceed the transmissible limit, and therefore, control is performed to reduce the number of quantization bits, cut off the variable-length encoding, etc. However, such control only succeeds in reducing the code amount by sacrificing the image quality after decoding. As a result of the aforementioned shuffling, there is a possibility, for example, that such control may be effected while processing the center portion of the screen. Since the probability is high that such control is performed on the blocks near the end of each unit, the blocking/shuffling circuit 41 operates in such a manner that the blocks entered near the end of each block are positioned at the edge of the screen. An example of such shuffling is shown in Fig.15.

In Fig.15, it can be seen that blocks with smaller numbers are clustered nearer to the center of the screen, while blocks with larger numbers are clustered on both sides of the screen. Furthermore, in Fig.15, which shows the shuffling with N = 5, none of any attention block and the four neighboring blocks belong to the same unit. When the block address of the kth block in the uth unit is denoted as (i, j), the shuffling shown in Fig.15 is expressed by the following equation.

$$i = \frac{90}{2} - (-1)^{[((k-1)N)/60]} \times \left[\frac{\left[\frac{(k-1) \cdot N}{60}\right] + 1}{2}\right]$$

$$j = \left[\frac{60+N}{2N}\right] - 1 \times N + 1 - (-1)^{\mathrm{mod}((k-1),(60/N))} \times N \times \left[\frac{\mathrm{mod}\,(k-1 \cdot \frac{60}{N})+1}{2}\right] + \mathrm{mod}\left[\left[\frac{(k-1)\,N}{60}\right] + u - 1, N\right]$$

For example, to find the address of the block C134, since u = 3 and k = 134,

$$i = 45 - (-1)^{11} \times [6] = 45 + 6 = 51$$

$$j = ([65/10] - 1] \times 5 + 1 - (-1)^{1} \times 5 \times 1 + \mathrm{mod}(11 + 3 - 1, 5) = 26 + 5 + 3 = 34$$

which gives the address (51, 34).

There are many examples of such shuffling, other than that described above, some of which are shown in Figs.16

to 20. In Figs.18 to 20, the block vertical address starts from the top of the screen; it has been confirmed by simulation that distortion is likely to occur on both sides of the screen, as in the case of Fig.15. The shuffling of Fig.19 is similar to that of Fig.18, except that N = 10, providing 10 units names A to K (I is not used as it can be confused with 1). Also, the shuffling of Fig.20 is similar to that of Fig.18, except that N = 3. The shuffing such as shown in Fig.18 is expressed by the following equation.

$$i = \frac{90}{2} - (-1)^{[[(k-1) \cdot N]/60]} \times \left[\frac{\left[\frac{(k-1) \cdot N}{60}\right] + 1}{2} \right]$$

$$j = N \times \mathrm{mod}\left(k - 1, \frac{60}{N}\right) + 1 + \mathrm{mod}\left[\frac{(k-1) \cdot N}{60}\right] + u - 1,$$

N For example, in Fig. 18, to find the address of the block E147, since u = 5 and k = 147,

$$i = 45 - (-1)^{12} \times [(12 + 1)/2] = 45 - 6 = 39$$

$$j = 5 \times 2 + 1 + \mathrm{mod}(12 + 5 - 1, 5) = 11 + 1 = 12$$

which gives the address (39, 12).

With the above-described shuffling, distortion resulting from the code amount control is driven to both sides of the screen. In the above equation, when N = 2, the possibility may arise that some of four neighboring blocks belong to the same unit, but this is the problem that arises as a result of the shuffling so performed as to position the blocks nearer to the sides of the screen as k increases. Since such blocks appear only on limited portions of the screen, they do not substantially affect the distribution of the code amount. In an ordinary digital VTR, this does riot present any problems in actual use since N is usually set at 3 or a greater number considering special replay modes, etc. In any of the above figures illustrating the shuffling, the operation is based on divisions with N as the modulus, but it will be appreciated that similar effects can be obtained when the divisions are performed by taking an integral multiple of N or a quotient of an integer by an integer of N as the modulus. For example, when N = 10, usually 10 is taken as the modulus, but either 20 or 5[10 × (1/2)] may be taken as the modulus.

In the above first and second embodiments, shuffling is performed in units of blocks, but alternatively, shuffling may be performed by, for example, grouping (t × s) blocks into one unit.

In the above embodiments, orthogonal transform has been described by taking the DCT as an example, but it will be appreciated that other orthogonal transforms than the DCT, such as Hadamard transform, K-L transform, etc. may also be used. Also, the weighting circuit 3 may be omitted in a configuration in which the quantization width of the quantizing circuit 4 is made to vary depending on the frequency.

Claims

1. A video signal encoding apparatus for compressing and encoding a digital video signal, comprising:

    block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality of pixels;
    transformation means for performing an orthogonal transform on each of the structured blocks to obtain a and encoding a digital video signal containing a chrominance signal, comprising:

        block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality of pixels;
        transformation means for performing an orthogonal transform on each of the structured blocks to obtain a transform coefficient;
        encoding means for encoding the obtained transform coefficient to obtain coded data; and
        unit structuring means for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, by shuffling the blocks in such a manner that any given shuffling unit and four shuffling units most adjacent to said given shuffling unit belong to different units, the reference of the shuffling unit being the size that the blocks of said chrominance signal occupy on the screen.

2. A video signal encoding apparatus for compressing and encoding a digital video signal, comprising:

block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality of pixels;

transformation means for performing an orthogonal transform on each of the structured blocks to obtain a transform coefficient;

encoding means for encoding the obtained transform coefficient to obtain coded data: and

unit structuring means for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, in such a manner that any given block and four blocks most adjacent to said given block belong to different units.

3. A video signal encoding apparatus for compressing and encoding a digital video signal, comprising:

block structuring means for structuring the video signal into a matrix array of blocks each consisting of a plurality of pixels;

transformation means for performing an orthogonal transform on each of the structured blocks to obtain a transform coefficient;

encoding means for encoding the obtained transform coefficient to obtain coded data;

unit structuring means for structuring units each comprising a plurality of blocks, prior to the orthogonal transform by said transformation means, in such a manner that any given block and four blocks most adjacent to said given block belong to different units;

decision means for deciding the order in which the blocks are to be encoded, the order within each unit being such that encoding is performed starting with the blocks nearer to the center of the screen and then proceeding to the blocks nearer to the sides of the screen; and

control means for controlling the amount of coded data on a unit-by-unit basis.

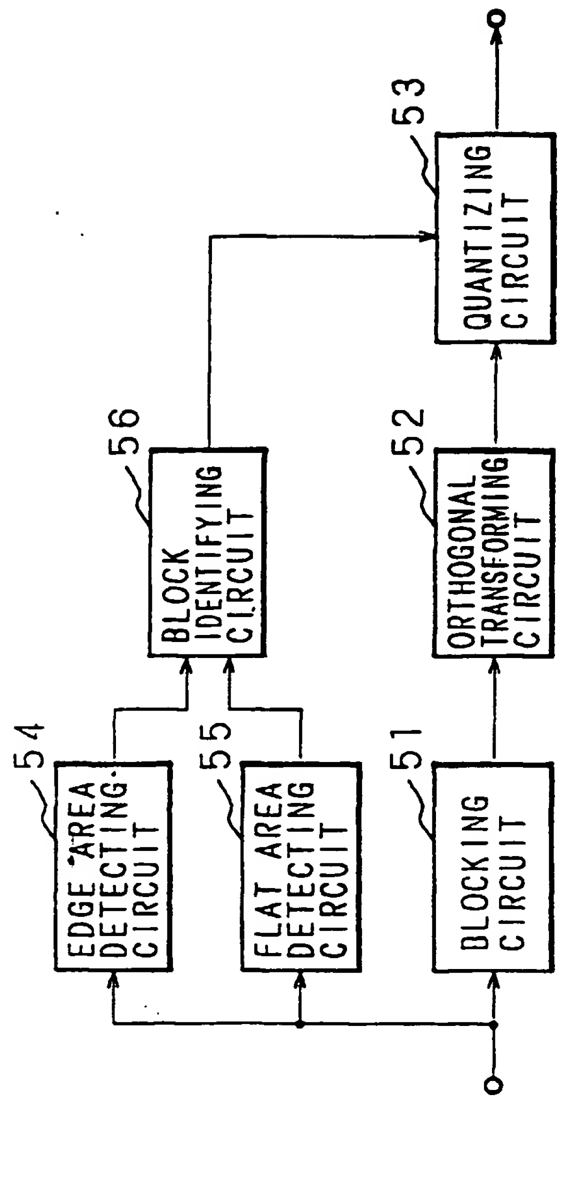
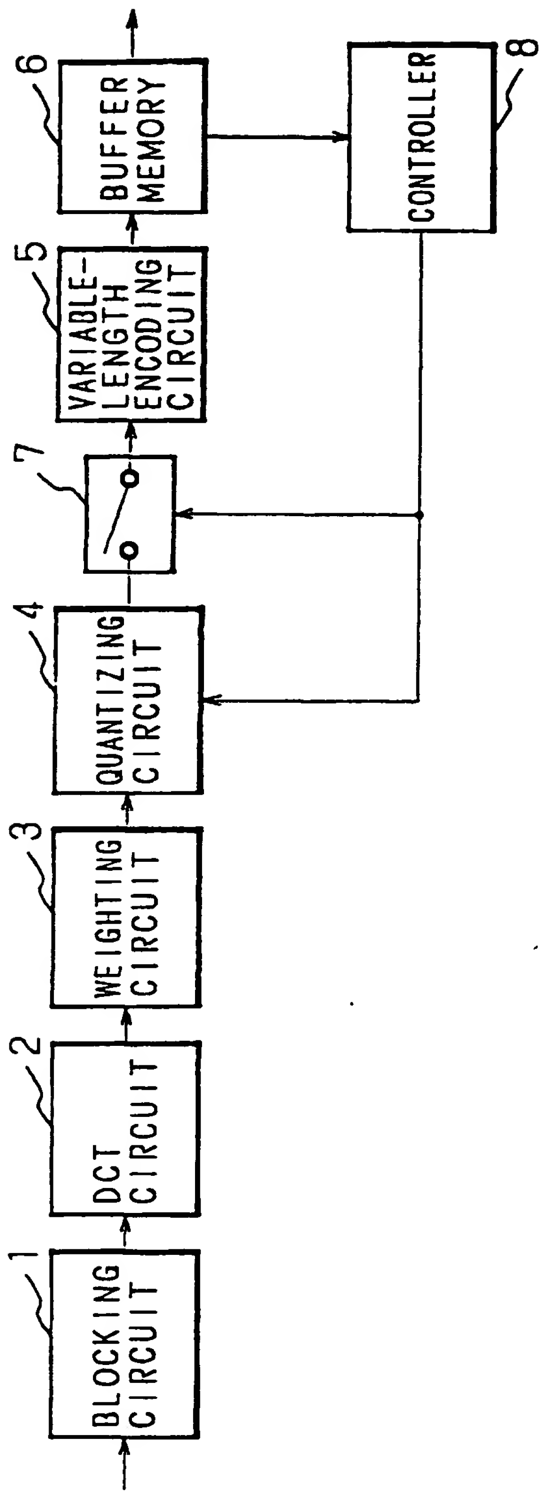


Fig. 1
Prior Art

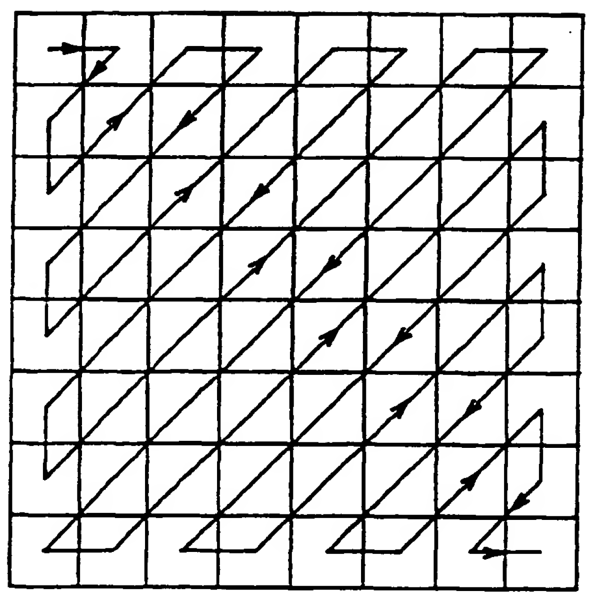

BLOCKING CIRCUIT
1
DCT CIRCUIT
2
WEIGHTING CIRCUIT
3
QUANTIZING CIRCUIT
4
7
VARIABLE-LENGTH ENCODING CIRCUIT
5
BUFFER MEMORY
6
CONTROLLER
8

F I g. 2

Fig. 3

80	3	0	2	1	0		
2	1	−1	0				
−1	0	1					
1	0						
0							

Fig. 4



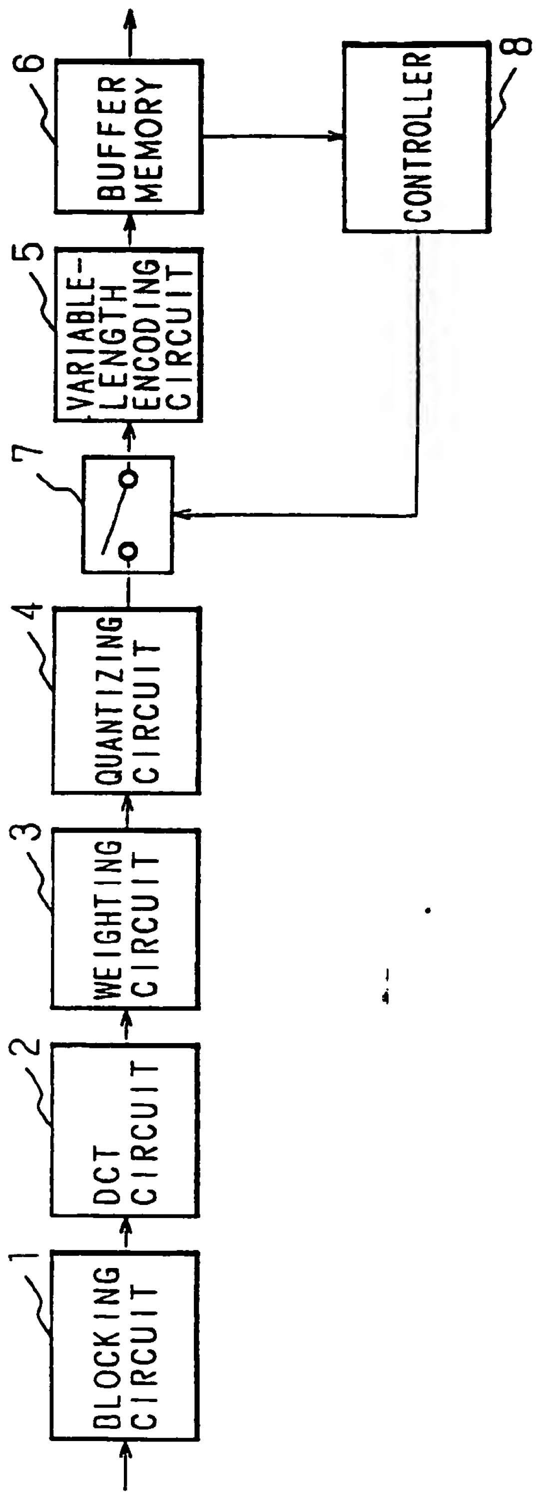

BLOCKING CIRCUIT
1
DCT CIRCUIT
2
WEIGHTING CIRCUIT
3
QUANTIZING CIRCUIT
4
7
VARIABLE-LENGTH ENCODING CIRCUIT
5
BUFFER MEMORY
6
CONTROLLER
8

Fig. 5

Fig. 6

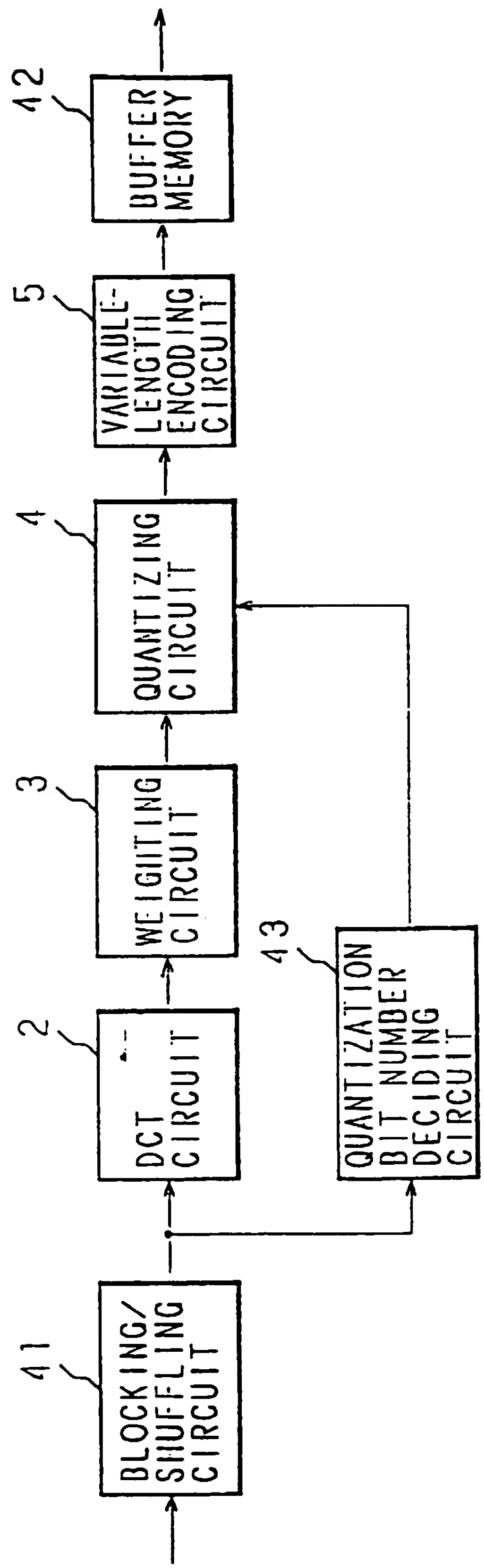

41
BLOCKING/
SHUFFLING
CIRCUIT
2
DCT
CIRCUIT
3
WEIGHTING
CIRCUIT
4
QUANTIZING
CIRCUIT
5
VARIABLE-
LENGTH
ENCODING
CIRCUIT
42
BUFFER
MEMORY
43
QUANTIZATION
BIT NUMBER
DECIDING
CIRCUIT

Fig. 7

n PIXELS

n PIXELS

A1	B1	C1	D1	E1	A2	B2	C2	D2	E2	A3	B3
E19	A19	B19	C19	D19	E20	A20	B20	C20	D20	E21	A21
D37	E37	A37	B37	C37	D38	E38	A38	B38	C38	D39	E39
C55	D55	E55	A55	B55	C56	D56	E56	A56	B56	C57	D57
B73	C73	D73	E73	A73	B74	C74	D74	E74	A74	B75	C75
A91	B91	C91	D91	E91	A92	B92	C92	D92	E92	A93	B93
E109	A109	B109	C109	D109	E110	A110	B110	C110	D110	E111	A111

Fig. 8

E	A	F
D	ATTENTION BLOCK	B
H	C	G

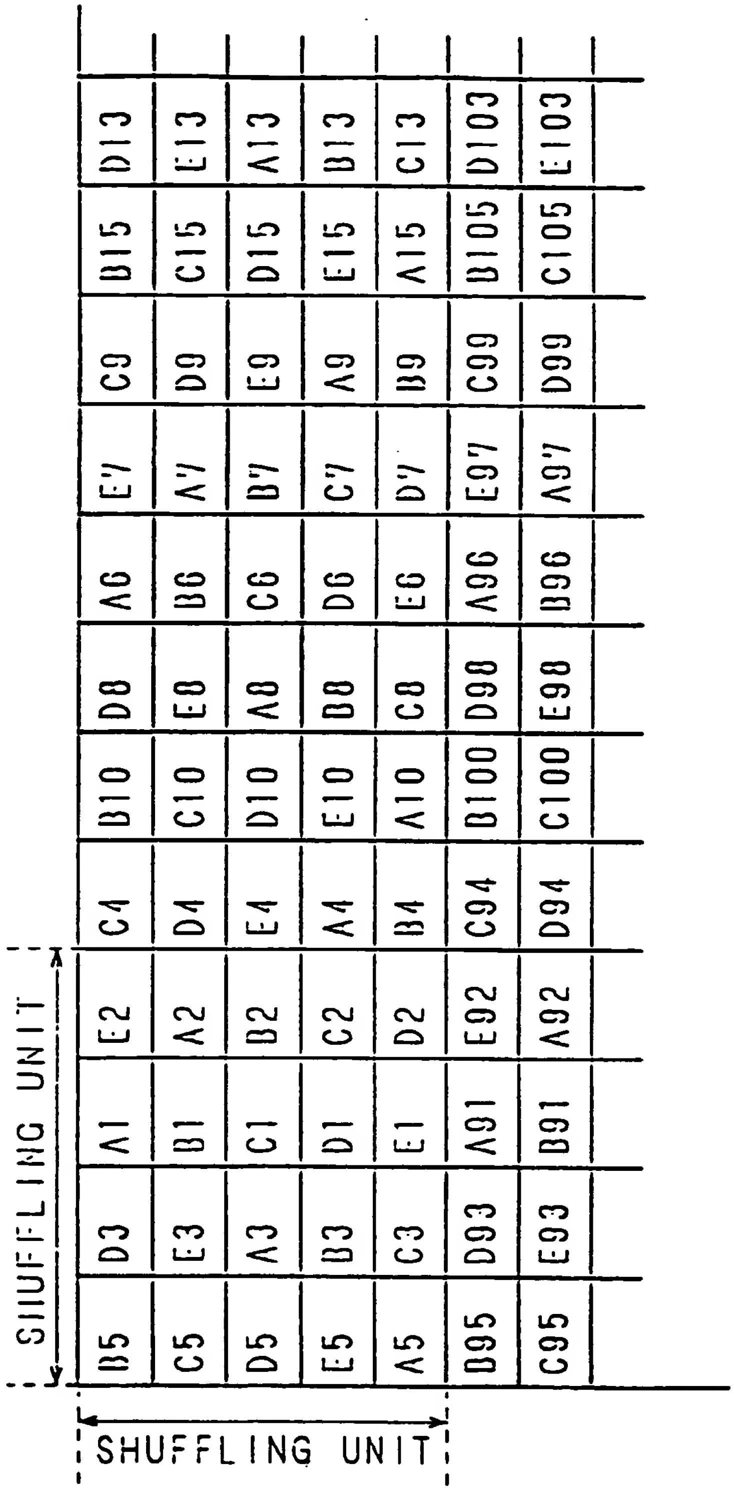

B5 D3 A1 E2 C4 B10 D8 A6 E7 C9 B15 D13
C5 E3 B1 A2 D4 C10 E8 B6 A7 D9 C15 E13
D5 A3 C1 B2 E4 D10 A8 C6 B7 E9 D15 A13
E5 B3 D1 C2 A4 E10 B8 D6 C7 A9 E15 B13
A5 C3 E1 D2 B4 A10 C8 E6 D7 B9 A15 C13
B95 D93 A91 E92 C94 B100 D98 A96 E97 C99 B105 D103
C95 E93 B91 A92 D94 C100 E98 B96 A97 D99 C105 E103
SHUFFLING UNIT
SHUFFLING UNIT

Fig. 9

Fig. 10

SHUFFLING UNIT

SHUFFLING UNIT

C4	D4	E4	A4	B4	C9	D9	E9	A9	B9	C14	D14
E2	A2	B2	C2	D2	E7	A7	B7	C7	D7	E12	A12
A1	B1	C1	D1	E1	A6	B6	C6	D6	E6	A11	B11
D3	E3	A3	B3	C3	D8	E8	A8	B8	C8	D13	E13
B5	C5	D5	E5	A5	B10	C10	D10	E10	A10	B15	C15
C94	D94	E94	A94	B94	C99	D99	E99	A99	B99	C104	D104
E92	A92	B92	C92	D92	E97	A97	B97	C97	D97	E102	A102

Fig. 11

SHUFFLING UNIT

SHUFFLING UNIT

E1	C2	D3	A4	B5	E6	C7	D8	A9	B10	E11	C12
C1	A2	E3	B4	D5	C6	A7	E8	B9	D10	C11	A12
A1	B2	C3	D4	E5	A6	B7	C8	D9	E10	A11	B12
B1	D2	A3	E4	C5	B6	D7	A8	E9	C10	B11	D12
D1	E2	B3	C4	A5	D6	E7	B8	C9	A10	D11	E12
E91	C92	D93	A94	B95	E96	C97	D98	A99	B100	E101	C102
C91	A92	E93	B94	D95	C96	A97	E98	B99	D100	C101	A102

Fig. 12

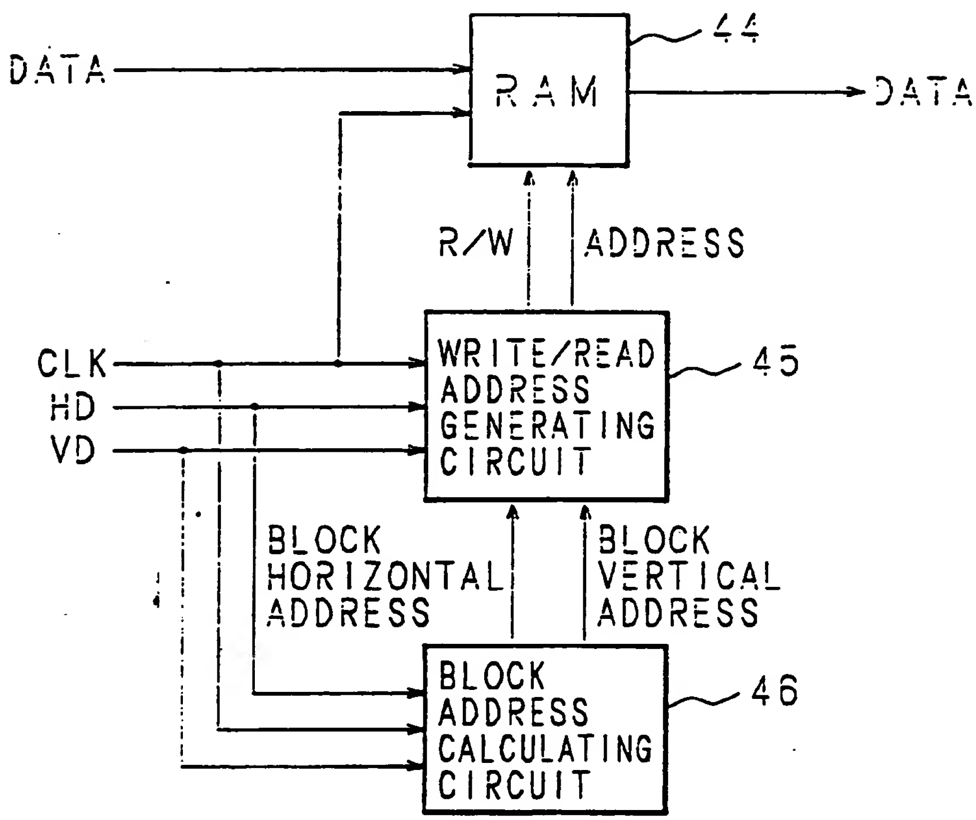

DATA
RAM
44
DATA
R/W
ADDRESS
CLK
HD
VD
WRITE/READ ADDRESS GENERATING CIRCUIT
45
BLOCK HORIZONTAL ADDRESS
BLOCK VERTICAL ADDRESS
BLOCK ADDRESS CALCULATING CIRCUIT
46

Fig. 13

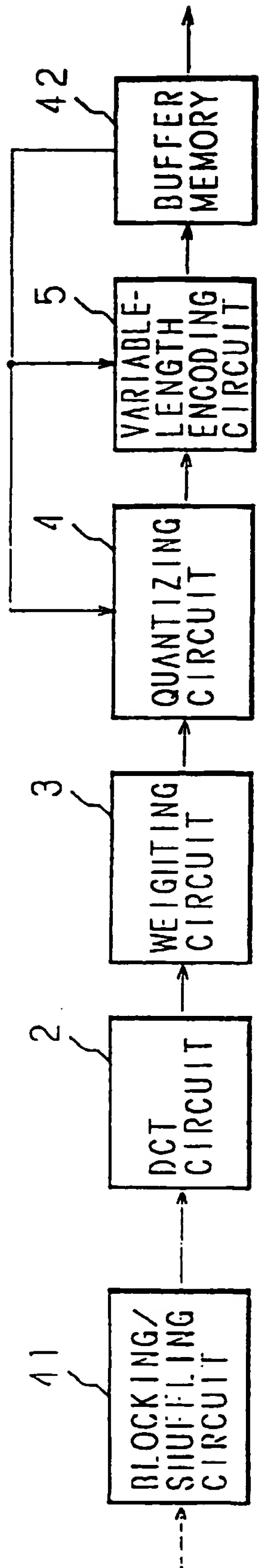
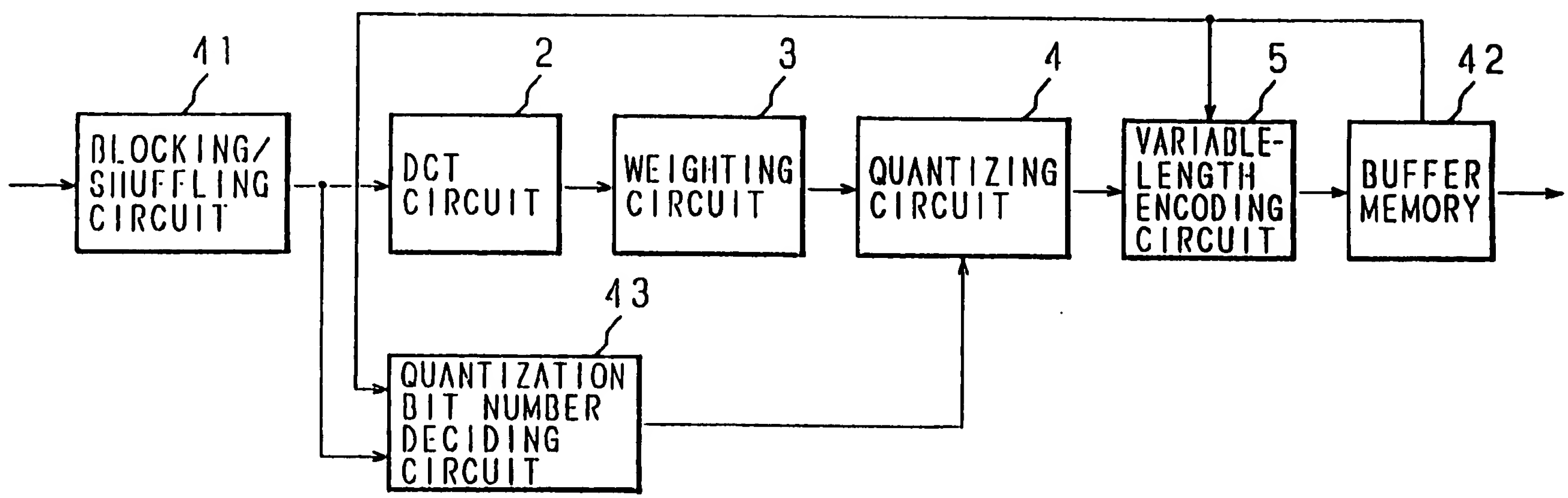

41
BLOCKING/ SHUFFLING CIRCUIT
2
DCT CIRCUIT
3
WEIGHTING CIRCUIT
4
QUANTIZING CIRCUIT
5
VARIABLE-LENGTH ENCODING CIRCUIT
42
BUFFER MEMORY

Fig. 14


41
BLOCKING/
SHUFFLING
CIRCUIT
2
DCT
CIRCUIT
3
WEIGHTING
CIRCUIT
4
QUANTIZING
CIRCUIT
5
VARIABLE-
LENGTH
ENCODING
CIRCUIT
42
BUFFER
MEMORY
43
QUANTIZATION
BIT NUMBER
DECIDING
CIRCUIT

F i g. 15

45

26

C147	E123	B99	D75	A51	C27	E3	D15	B39'	E63	C87	A111	D135	B159
D145	A121	C97	E73	B49	D25	A1	E13	C37	A61	D85	B109	E133	C157
E145	B121	D97	A73	C49	E25	B1	A13	D37	B61	E85	C109	A133	D157
A145	C121	E97	B73	D49	A25	C1	B13	E37	C61	A85	D109	B133	E157
B145	D121	A97	C73	E49	B25	D1	C13	A37	D61	B85	E109	C133	A157
C145	E121	B97	D73	A49	C25	E1	D13	B37	E61	C85	A109	D133	B157
D146	A122	C98	E74	B50	D26	A2	E14	C38	A62	D86	B110	E134	C158
E146	B122	D98	A74	C50	E26	B2	A14	D38	B62	E86	C110	A134	D158
A146	C122	E98	B74	D50	A26	C2	B14	E38	C62	A86	D110	B134	E158
B146	D122	A98	C74	E50	B26	D2	C14	A38	D62	B86	E110	C134	A158
C146	E122	B98	D74	A50	C26	E2	D14	B38	E62	C86	A110	D134	B158
D148	A124	C100	E76	B52	D28	A4	E16	C40	A64	D88	B112	E136	C160

Fig. 16

C147	E123	B99	D75	A51	C27	E3	C15	A39	D63	B87	E111	C135	A159
D145	A121	C97	E73	B49	D25	A1	D13	B37	E61	C85	A109	D133	B157
E145	B121	D97	A73	C49	E25	B1	E13	C37	A61	D85	B109	E133	C157
A145	C121	E97	B73	D49	A25	C1	A13	D37	B61	E85	C109	A133	D157
B145	D121	A97	C73	E49	B25	D1	B13	E37	C61	A85	D109	B133	E157
C145	E121	B97	D73	A49	C25	E1	C13	A37	D61	B85	E109	C133	A157
D146	A122	C98	E74	B50	D26	A2	D14	B38	E62	C86	A110	E134	B158
E146	B122	D98	A74	C50	E26	B2	E14	C38	A62	D86	B110	A134	C158
A146	C122	E98	B74	D50	A26	C2	A14	D38	B62	E86	C110	B134	D158
B146	D122	A98	C74	E50	B26	D2	B14	E38	C62	A86	D110	C134	E158
C146	E122	B98	D74	A50	C26	E2	D14	A38	D62	B86	E110	D134	A158
D148	A124	C100	E76	B52	D28	A4	D16	B40	E64	C88	A112	E136	B160

Fig. 17

B147	E123	C99	A75	D51	B27	E3	C15	A39	D63	B87	E111	C135	A159
C145	A121	D97	B73	E49	C25	A1	D13	B37	E61	C85	A109	D133	B157
D145	B121	E97	C73	A49	D25	B1	E13	C37	A61	D85	B109	E133	C157
E145	C121	A97	D73	B49	E25	C1	A13	D37	B61	E85	C109	A133	D157
A145	D121	B97	E73	C49	A25	D1	B13	E37	C61	A85	D109	B133	E157
B145	E121	C97	A73	D49	B25	E1	C13	A37	D61	B85	E109	C133	A157
C146	A122	D98	B74	E50	C26	A2	D14	B38	E62	C86	A110	D134	B158
D146	B122	E98	C74	A50	D26	B2	E14	C38	A62	D86	B110	E134	C158
E146	C122	A98	D74	B50	E26	C2	A14	D38	B62	E86	C110	A134	D158
A146	D122	B98	E74	C50	A26	D2	B14	E38	C62	A86	D110	B134	E158
B146	E122	C98	A74	D50	B26	E2	C14	A38	D62	B86	E110	C134	A158
C148	A124	D100	B76	E52	C28	A4	D16	B40	E64	C88	A112	D136	B160

Fig. 18

B145	A121	C97	E73	B49	D25	A1	E13	C37	A61	D85	B109	E133	C157
E145	B121	D97	A73	C49	E25	B1	A13	D37	B61	E85	C109	A133	D157
A145	C121	E97	B73	D49	A25	C1	B13	E37	C61	A85	D109	B133	E157
B145	D121	A97	C73	E49	B25	D1	C13	A37	D61	B85	E109	C133	A157
C145	E121	B97	D73	A49	C25	E1	D13	B37	E61	C85	A109	D133	B157
D146	A122	C98	E74	B50	D26	A2	E14	C38	A62	D86	B110	E134	C158
E146	B122	D98	A74	C50	E26	B2	A14	D38	B62	E86	C110	A134	D158
A146	C122	E98	B74	D50	A26	C2	B14	E38	C62	A86	D110	B134	E158
B146	D122	A98	C74	E50	B26	D2	C14	A38	D62	B86	E110	C134	A158
C146	E122	B98	D74	A50	C26	E2	D14	B38	E62	C86	A110	D134	B158
D147	A124	C99	E75	B51	D27	A3	E15	C38	A63	D87	B111	E135	C159
E147	B124	D99	A75	C51	E27	B3	A15	D38	B63	E87	C111	A135	D159

Fig. 19

J73	A61	C49	E37	G25	J13	A1	K7	H19	F31	D43	B55	K67	H79
K73	B61	D49	F37	H25	K13	B1	A7	J19	G31	E43	C55	A67	J79
A73	C61	E49	G37	J25	A13	C1	B7	K19	H31	F43	D55	B67	K79
B73	D61	F49	H37	K25	B13	D1	C7	A19	J31	G43	E55	C67	A79
C73	E61	G49	J37	A25	C13	E1	D7	B19	K31	H43	F55	D67	B79
D73	F61	H49	K37	B25	D13	F1	E7	C19	A31	J43	G55	E67	C79
E73	G61	J49	A37	C25	E13	G1	F7	D19	B31	K43	H55	F67	D79
F73	H61	K19	B37	D25	F13	H1	G7	E19	C31	A43	J55	G67	E79
G73	J61	A49	C37	E25	G13	J1	H7	F19	D31	B43	K55	H67	F79
H73	K61	B49	D37	F25	H13	K1	J7	G19	E31	C43	A55	J67	G79
J74	A62	C50	E38	G26	J14	A2	K8	H20	F32	D44	B55	K68	H80
K74	B62	D50	F38	H26	K14	B2	A8	J20	G32	E44	C55	A68	J80

Fig. 20

A241	C201	B161	A121	C81	B41	A1	C21	A61	B101	C141	A181	B221	C261
B241	A201	C161	B121	A81	C41	B1	A21	B61	C101	A141	B181	C221	A261
C241	B201	A161	C121	B81	A41	C1	B21	C61	A101	B141	C181	A221	B261
A242	C202	B162	A122	C82	B42	A2	C22	A62	B102	C142	A182	B222	C262
B242	A202	C162	B122	A82	C42	B2	A22	B62	C102	A142	B182	C222	A262
C242	B202	A162	C122	B82	A42	C2	B22	C62	A102	B142	C182	A222	B262
A243	C203	B163	A123	C83	B43	A3	C23	A63	B103	C143	A183	B223	C263
B243	A203	C163	B123	A83	C43	B3	A23	B63	C103	A143	B183	C223	A263
C243	B203	A163	C123	B83	A43	C3	B23	C63	A103	B143	C183	A223	B263
A244	C204	B164	A124	C84	B44	A4	C24	A64	B104	C144	A184	B224	C264
B244	A204	C164	B124	A84	C44	B4	A24	B64	C104	A144	B184	C224	A264
C244	B204	A164	C124	B84	A44	C4	B24	C64	A104	B144	C184	A224	B264